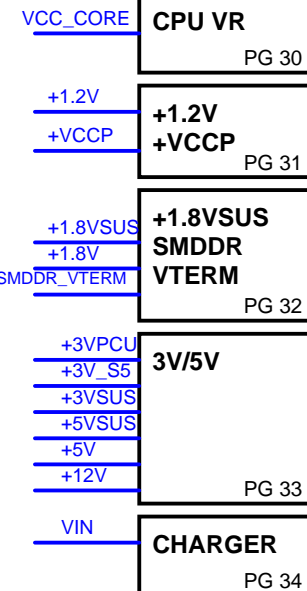


BOM MARK
SA@ SATA 要打
PA@ PATA 要打
3@ 3G 要打

ZH3

ZH3 ASSY P/N :31ZH3MB0008
ZH3 MB C/S ASSY P/N: 41ZH3CS0001
ZH3 MB S/S ASSY P/N: 51ZH3SS0003



DDRII-SODIMM1 PG 7,8

DDRII-SODIMM2 PG 7,8

AMD S1
Turion 64 Rev.F Dual-Core/
Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

CPU THERMAL
SENSOR
Page 5

DVI
TI TFP513PAP
Page : 29

DVI

Docking
Page : 30

EXT CRT

DVO

TVOUT

RGB

LVDS

CRT Switch
SN74CBTLV3257PWR
Page : 16

INT CRT

CRT
Page : 16

LVDS
Page : 16

Mini Card (WLAN) PCIE3 & USB4
PCI Express Mini Card PG 19

PCI-E, 1X

Express Card PCIE2 & USB5
NEW CARD PG 31

PCI-E, 1X

USB 2.0 * 1(USB5)

RS485
465 FCBGA
PG 9,10,11,12

A_LINK

SATA - HDD PG 23

SATA0

PATA - HDD PG 23

PATA 100

SB460
549 BGA
PG 14,15,16,17

USB2.0 (P0~P7)

Bluetooth
USB7 PG 20

USB2.0 I/O Port X3
USB0 & USB1 & USB2 PG 20

DSC USB I/F
USB6 PG 16

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz

REF 14MHz

CLOCK GENERATOR
ICS951462
PG 2

PCI Bus 33MHz

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
5788M	AD20	REQ2# / GNT2#	INT G#

AD25
REQ0# / GNT0#
INT E/F/G#

OSC
48MHZ

BROADCOM
10/100/1G LAN
5788M PG 17

BOTH HAND
TRANSFORMER PG 18

RJ45
PG 18

Azalia Audio
PG 24

Amplifier
MAX4411 PG 25

Amplifier
MAX9755A PG 25

Azalia MDC
PG 24

MIC.
PG 25

H.P/SPDIF
PG 25

INT.
S.P.
PG 25

MODEM
RJ 11
PG 18

G-SENSOR
KXP84-0200
Page : 23

KBC
NS97551
PG 27

NS
SIO (87383)
Page : 26

K/B
CONN.
PG 28

Touch
Pad
PG 28

Flash
ROM
PG 27

FIR
Page : 26

X-Bus

TI
PCMCIA+1394
+6 IN 1
PCI7412
Page : 21~22

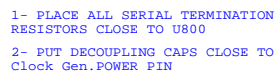
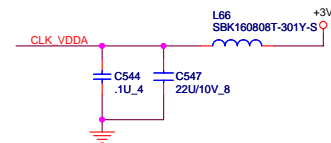
1394
Page: 21

5 IN 1
Page: 22

PCMCIA
Page: 22



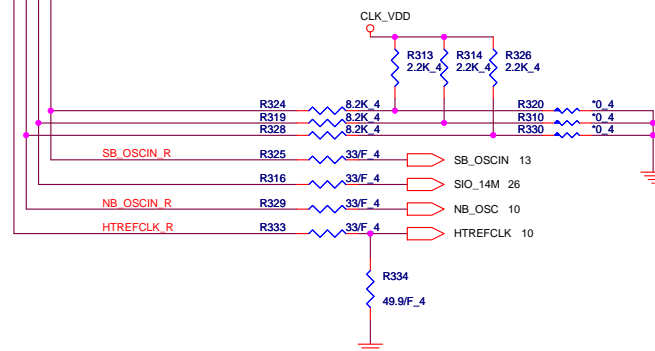
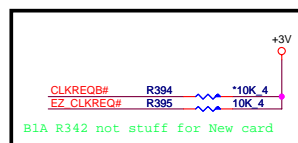
PROJECT :ZH3
Quanta Computer Inc.



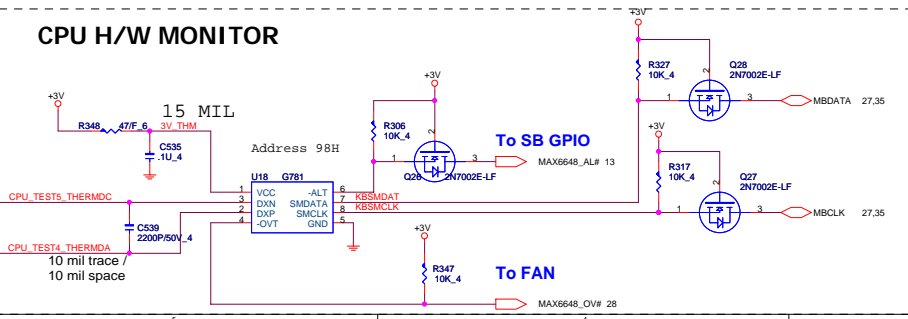
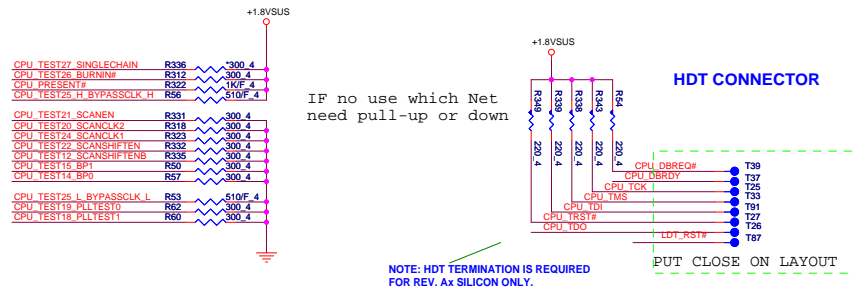
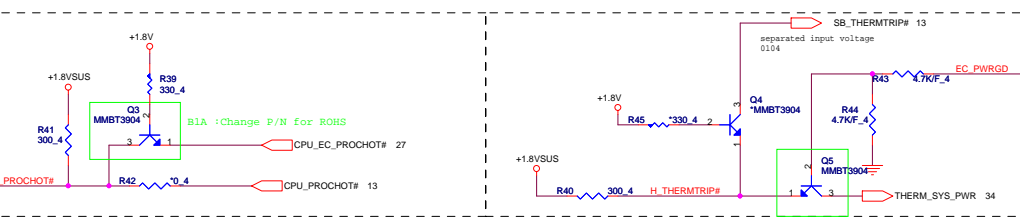
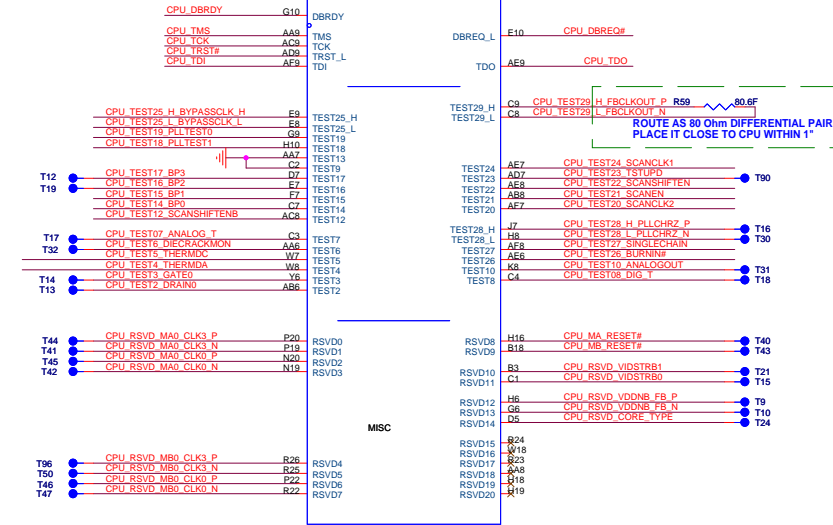
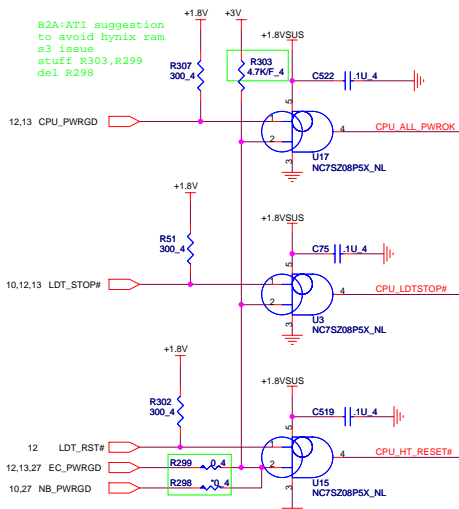
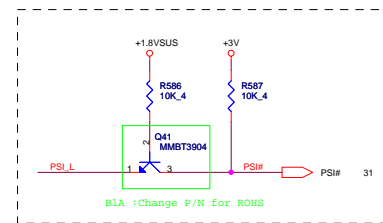
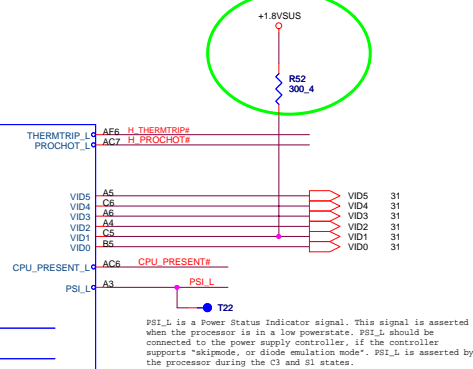
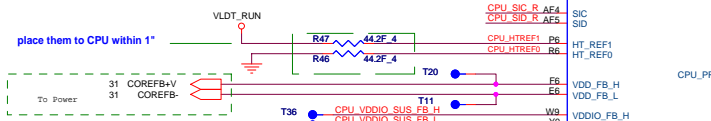
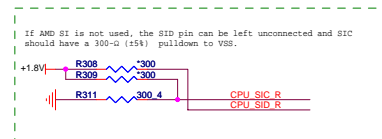
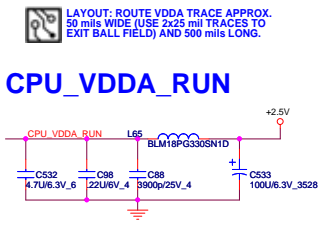
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

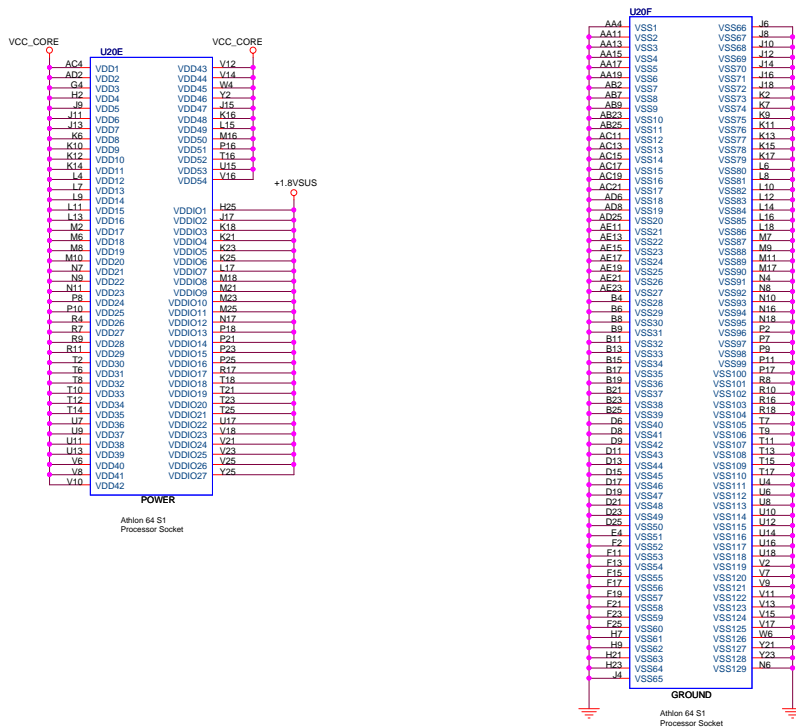
Check AMD clock

```
CLKREQA# Controls SRC5,6,7
CLKREQB# Controls SRC2,3,4,ATIG3
CLKREQC# Controls SRC0,1,ATIG0,1,2
```

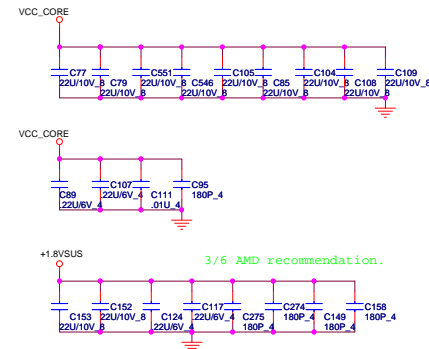


ATHLON Control and Debug

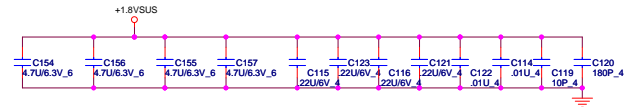




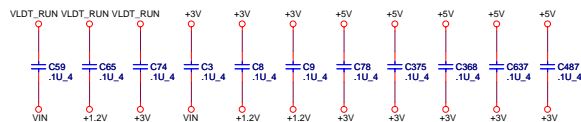
BOTTOMSIDE DECOUPLING



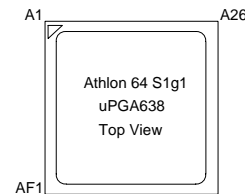
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



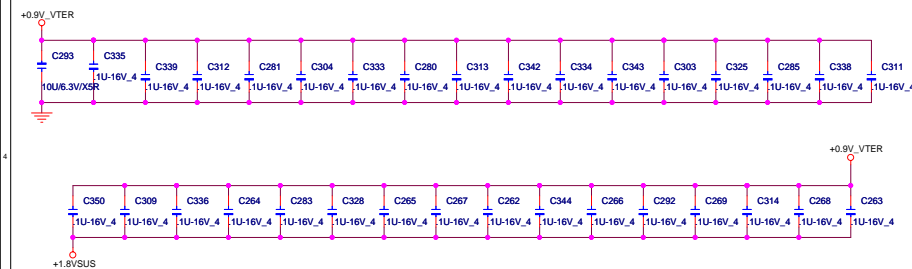
PROCESSOR POWER AND GROUND



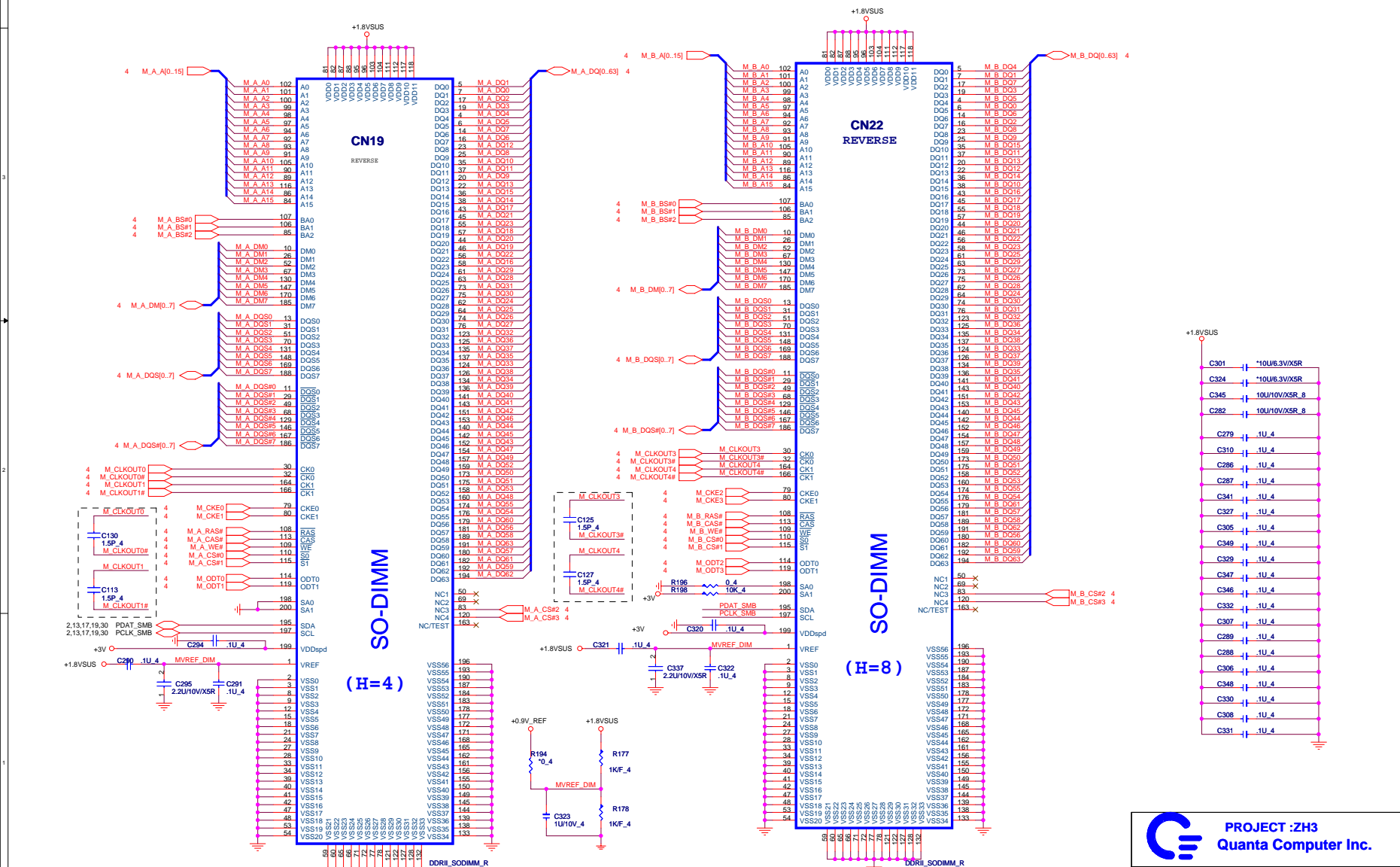
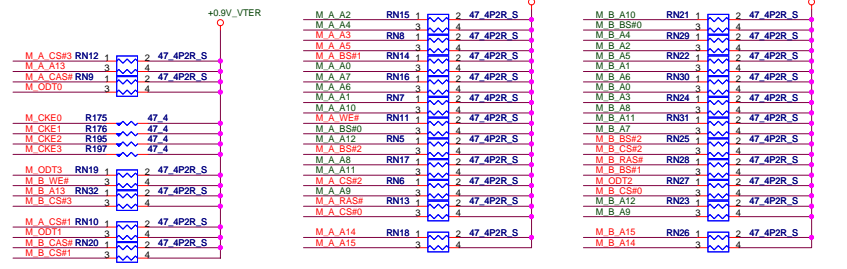
3/6 :ADD 0.1u CAPACITOR TO CROSS POWER PLANE.

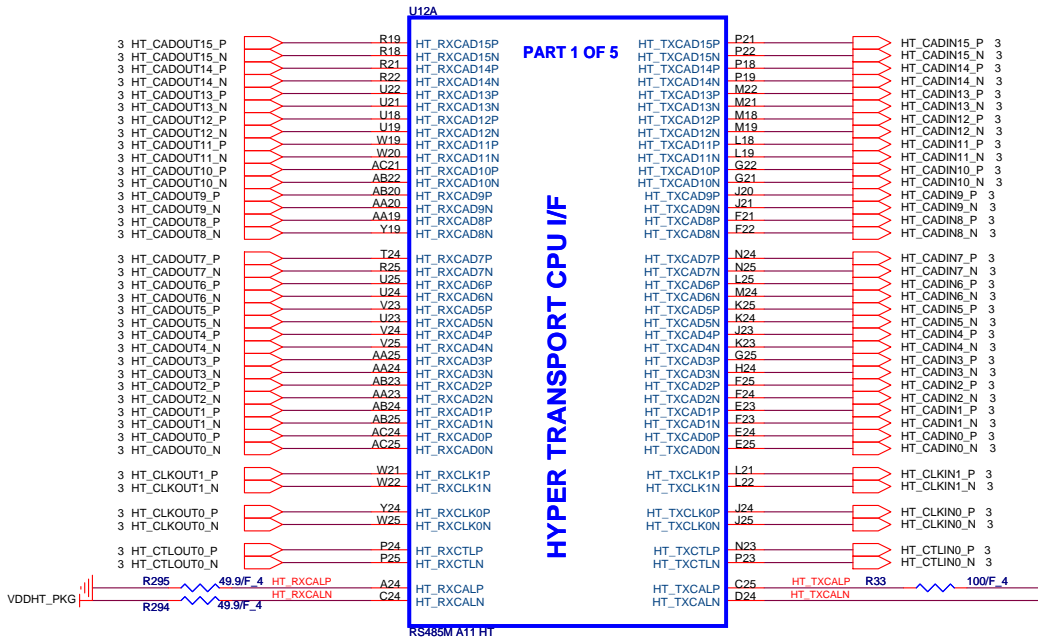


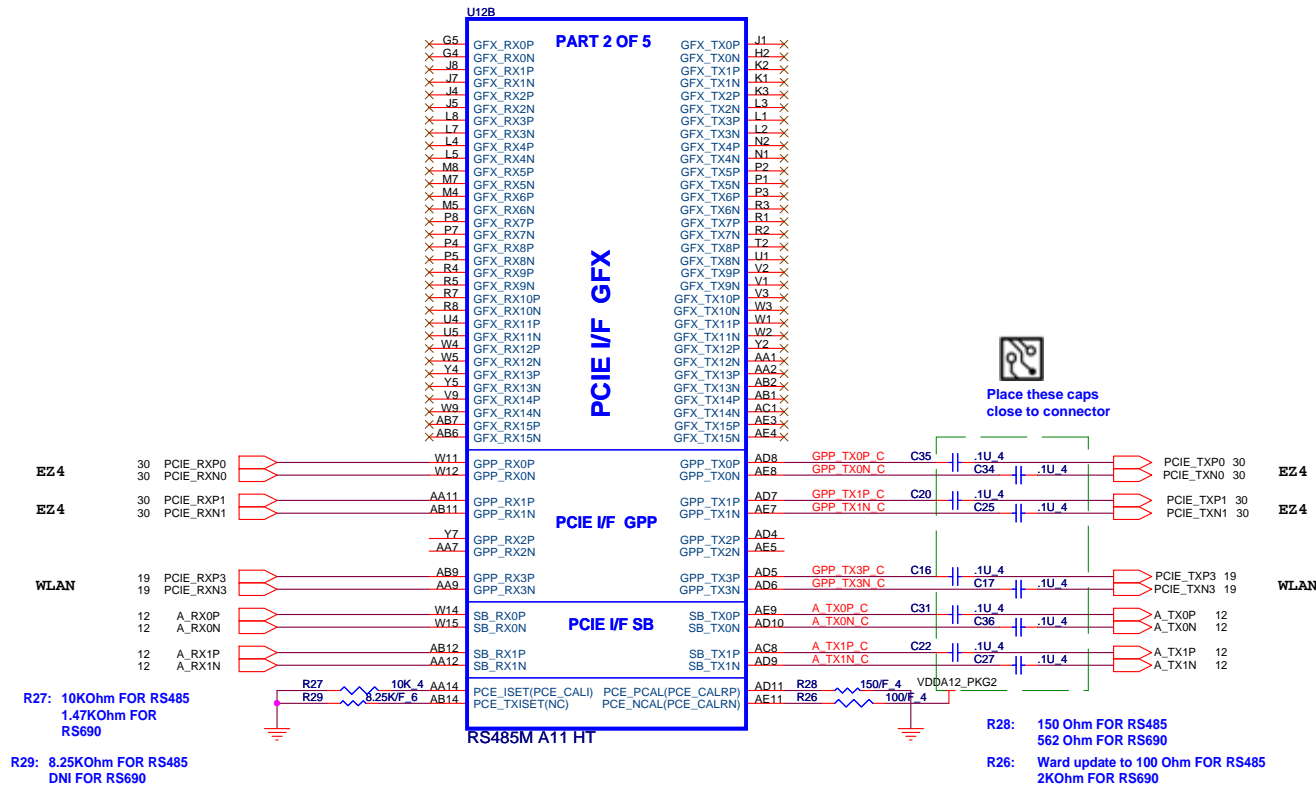
TERMINATOR DECOUPLING CAPACITOR

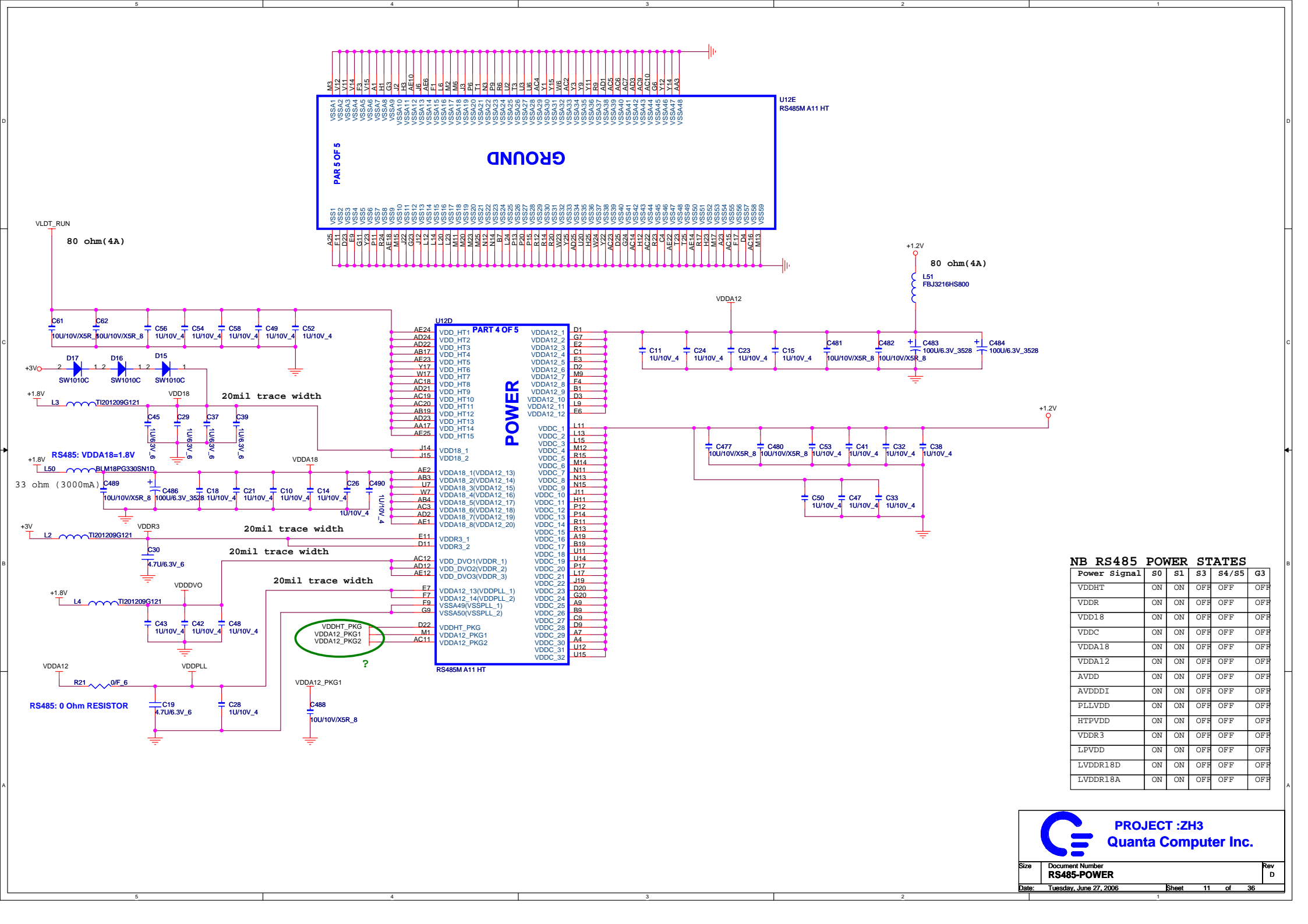


DDR2 TERMINATOR



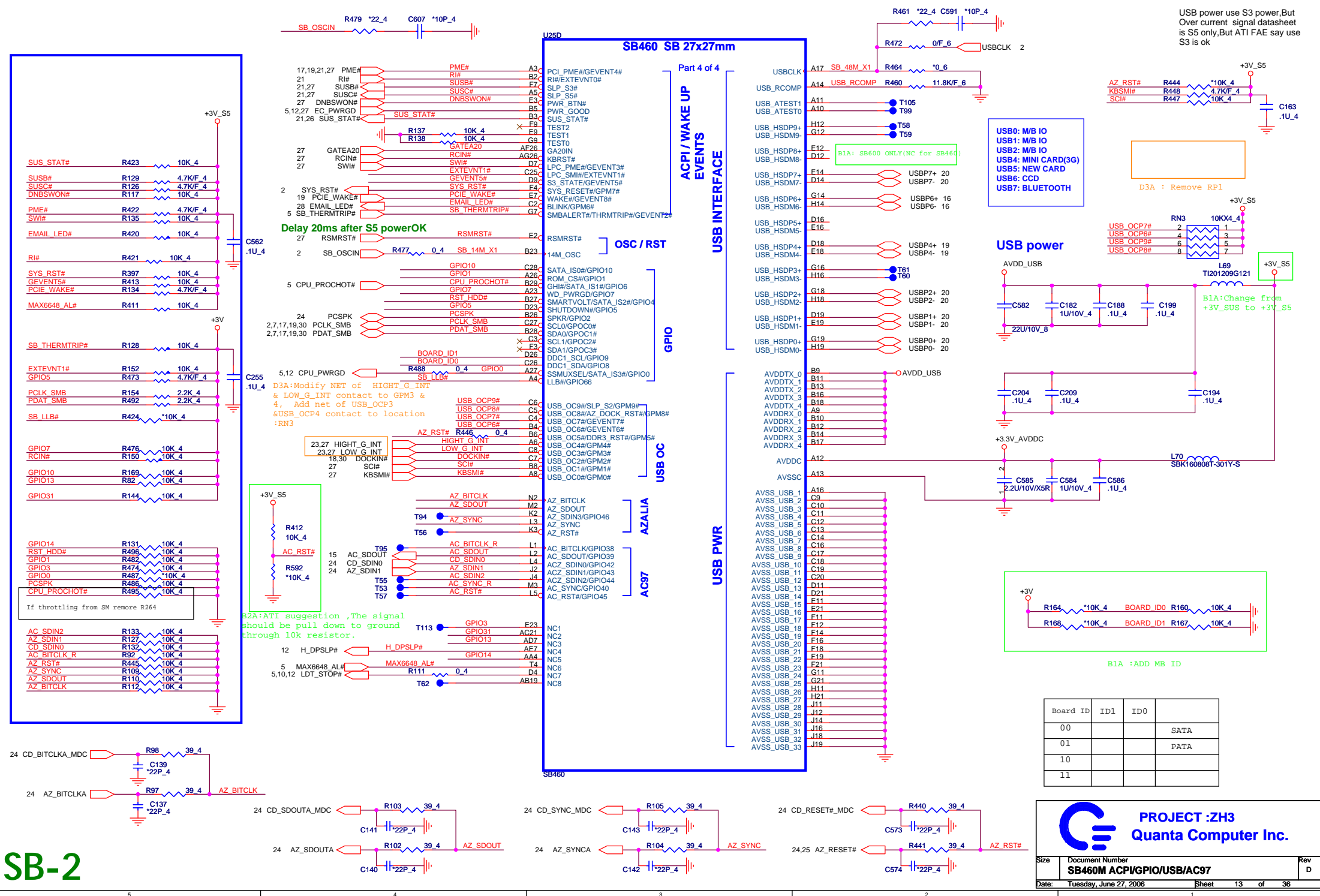







NB RS485 POWER STATES					
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDCC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

SB-2



Board ID	ID1	ID0	
00			SATA
01			PATA
10			
11			



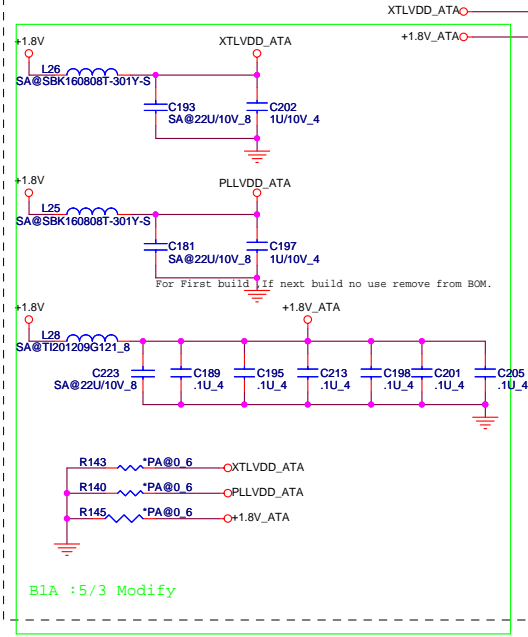
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev D
	SB460M ACPI/GPIO/USB/AC97	
Date:	Tuesday, June 27, 2006	Sheet 13 of 36

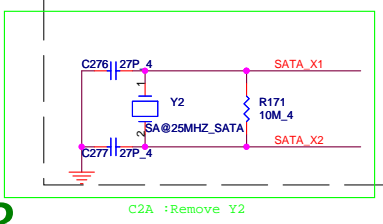
SB-3

WWW.AliSaler.Com

SATA Power



SATA clock



SB460 SB 27x27mm

Part 2 of 4

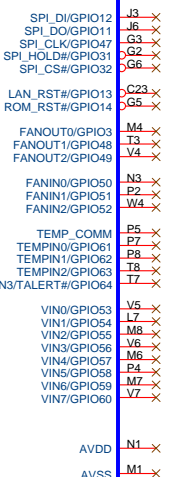
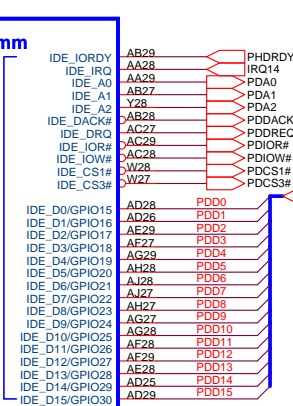
SERIAL ATA

ATA 66/100

SPI ROM

HW MONITOR

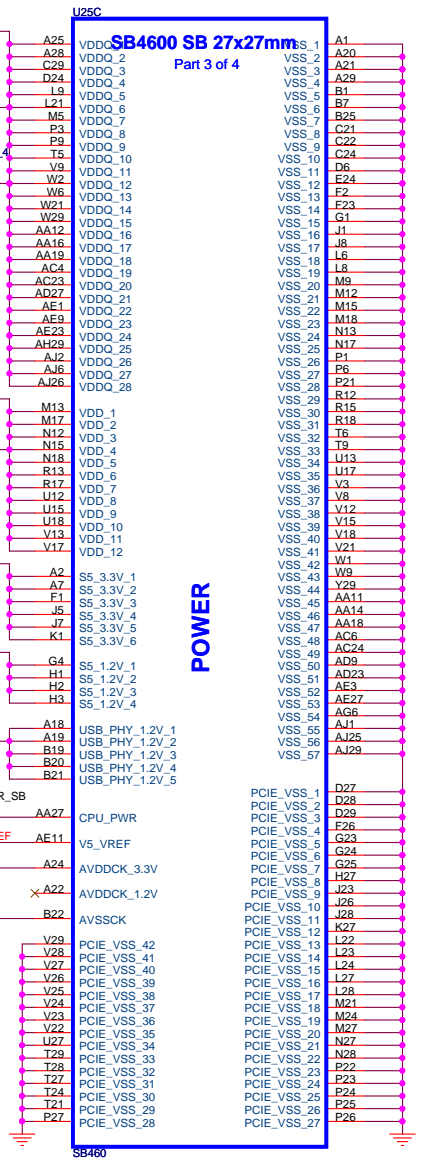
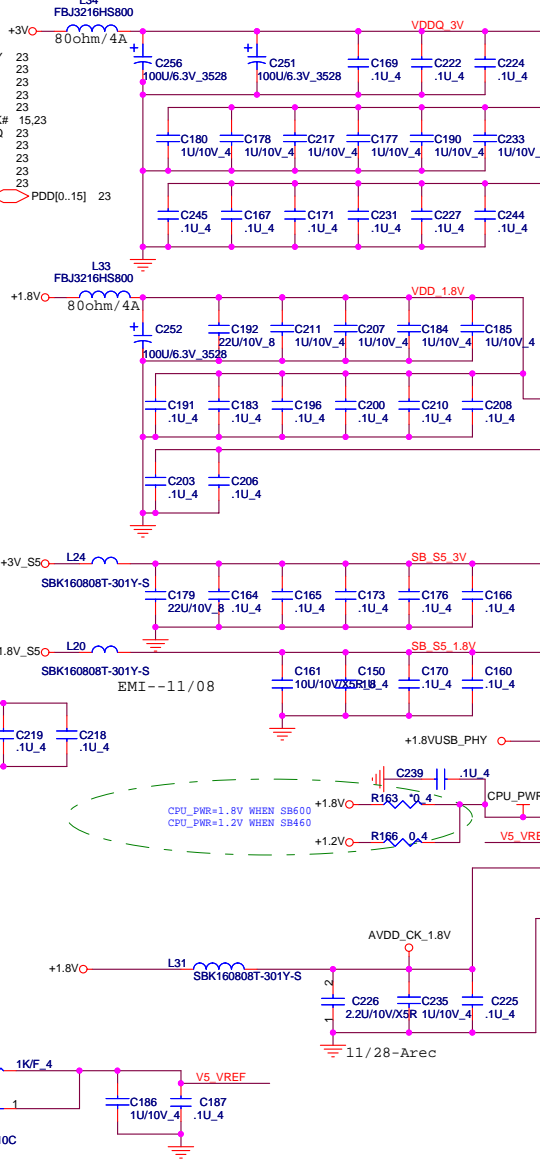
SERIAL ATA POWER



SB4600 SB 27x27mm

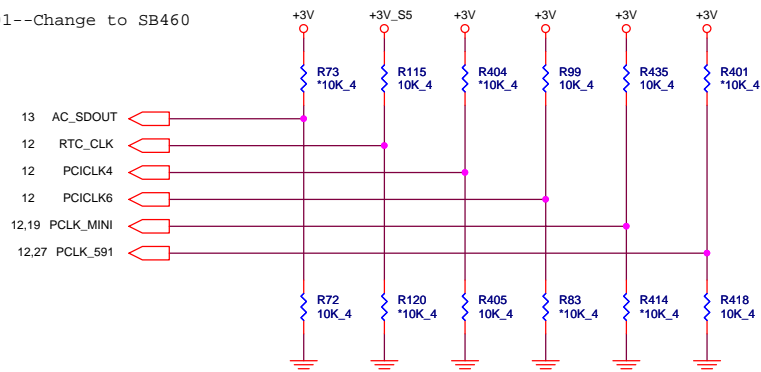
Part 3 of 4

POWER



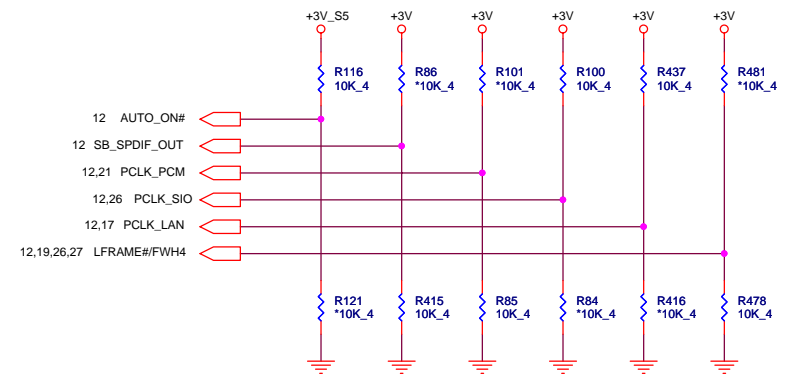
PROJECT : ZH3
Quanta Computer Inc.

Size	Document Number	Rev
	SB450M HDD/POWER/DECOUPLING	D
Date:	Tuesday, June 27, 2006	Sheet 14 of 36

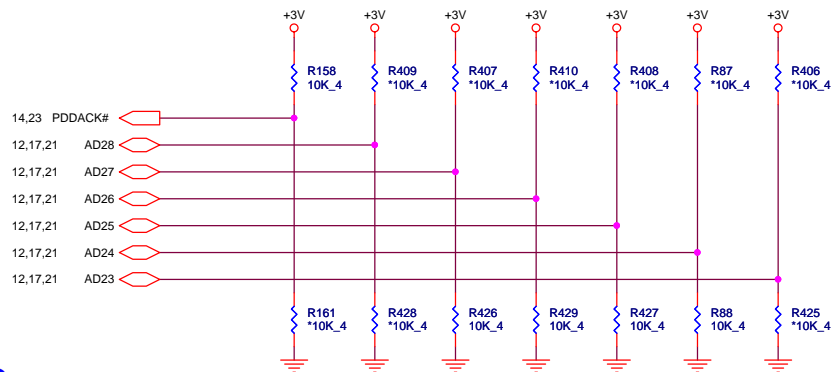


REQUIRED STRAPS

					PCLK_MINI	PCLK_591
PULL HIGH	AC_SDOUT USE DEBUG STRAPS	RTC_CLK INTERNAL RTC DEFAULT	PCI_CLK4 USE INT. PLL48	PCI_CLK6 CPU IF=K8	PCI_CLK0 ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM	PCI_CLK1 DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	



	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
PULL HIGH	ACPWRON MANUAL PWR ON DEFAULT	SPDIF_OUT SIO 24MHz	PCI_CLK2 XTAL MODE NOT SUPPORTED	PCI_CLK3 USB PHY POWERDOWN DISABLE DEFAULT	PCI_CLK5 PCIE_CM_SET LOW DEFAULT	LFRAME# ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH BIOS ENABLE	DISABLE THERMTRIP# AFTER STARTUP



DEBUG STRAPS

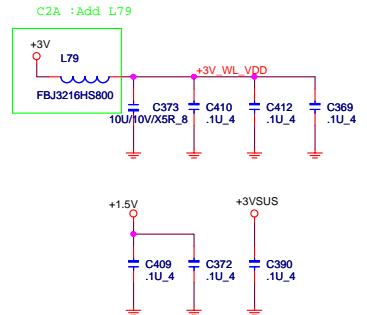
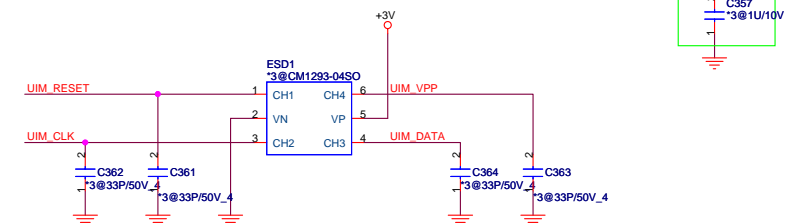
	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



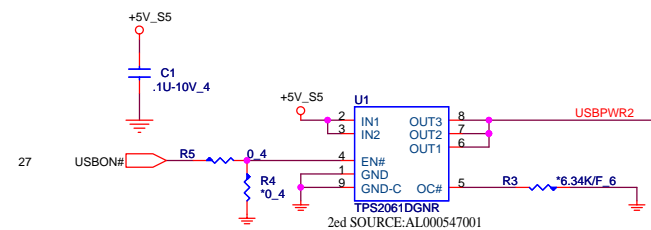
PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev D
	SB460M STRAPS	
Date:	Tuesday, June 27, 2006	Sheet 15 of 36

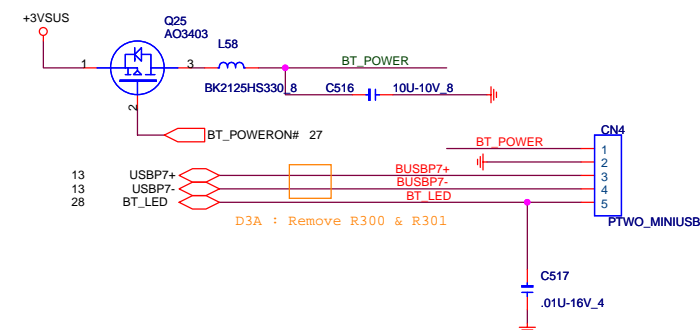
BIa:These signals of reserve have be used by wireless module of Foxconn BG. These signals impact LPC. I remove signal line in order to solve the WLAN issue.

[illegible]

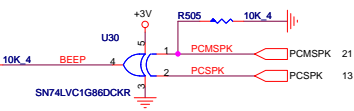
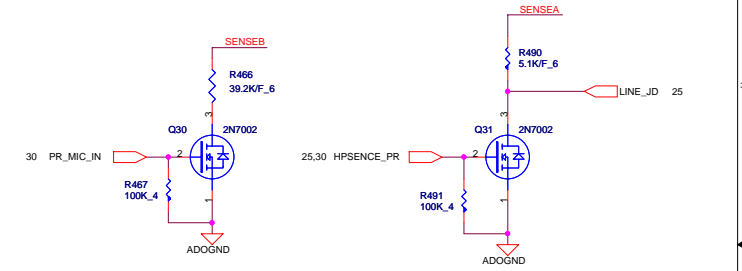
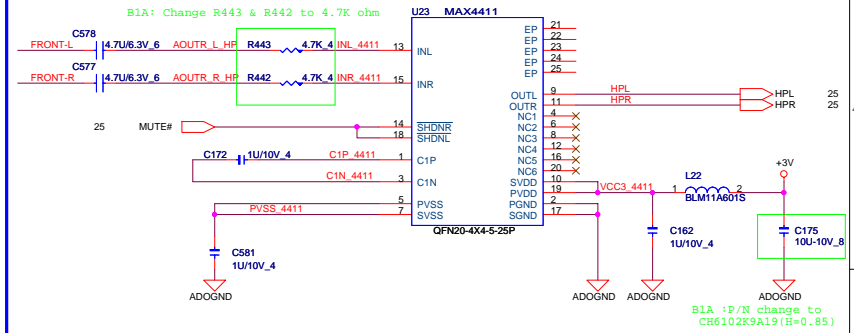
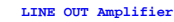
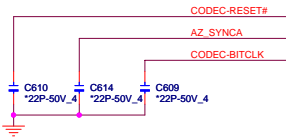
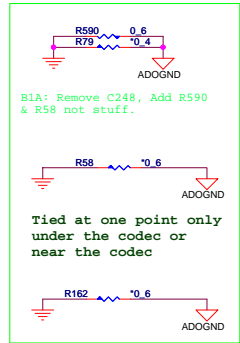
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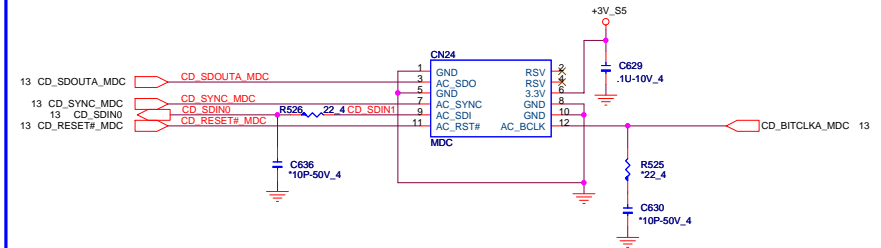
BLUETOOTH MODULE CONNECTOR



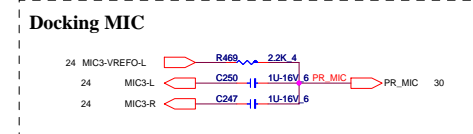
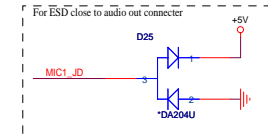
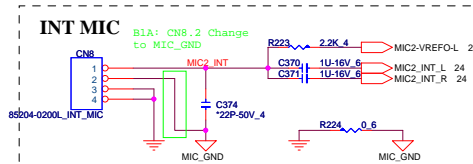
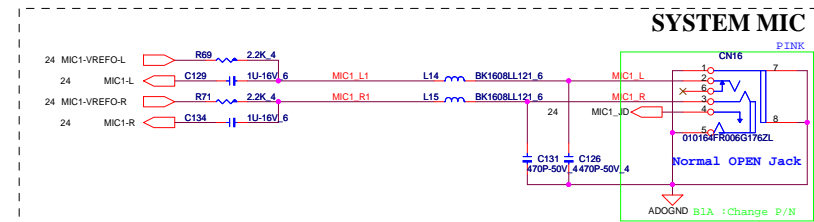
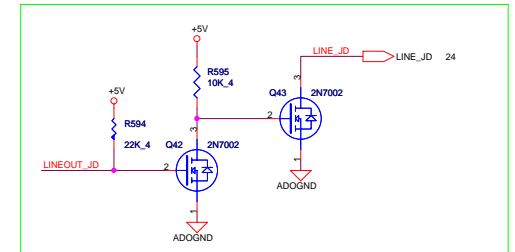
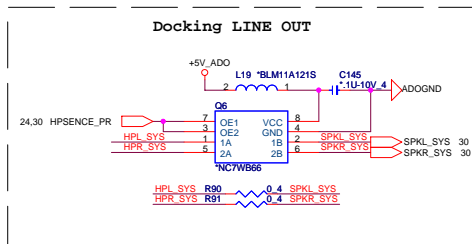
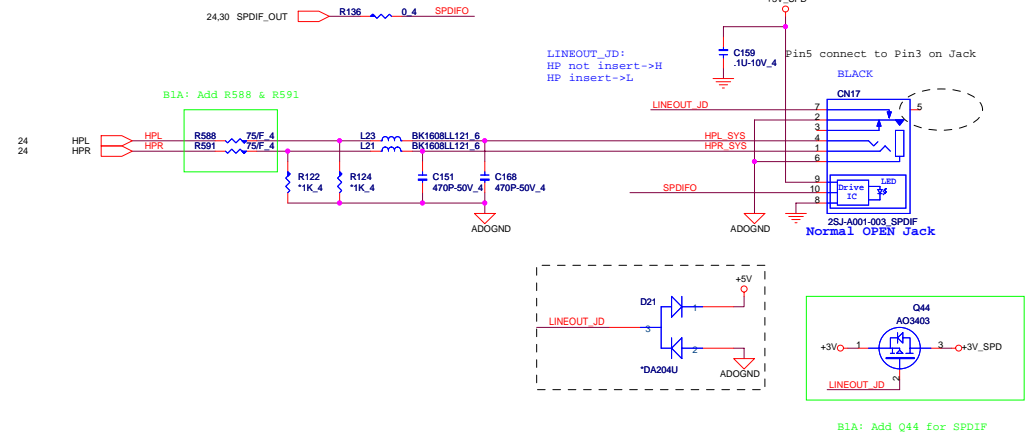
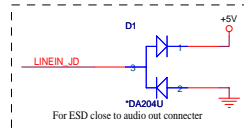
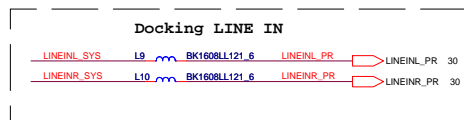
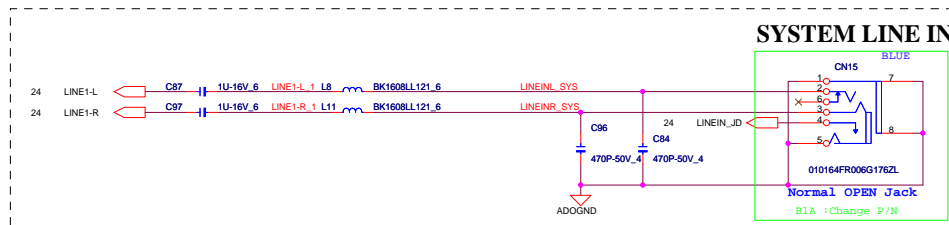
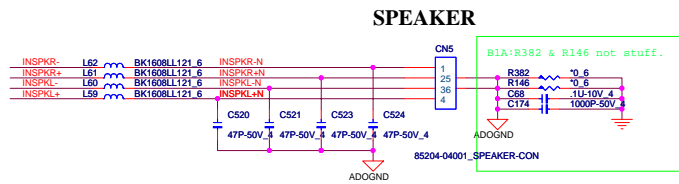
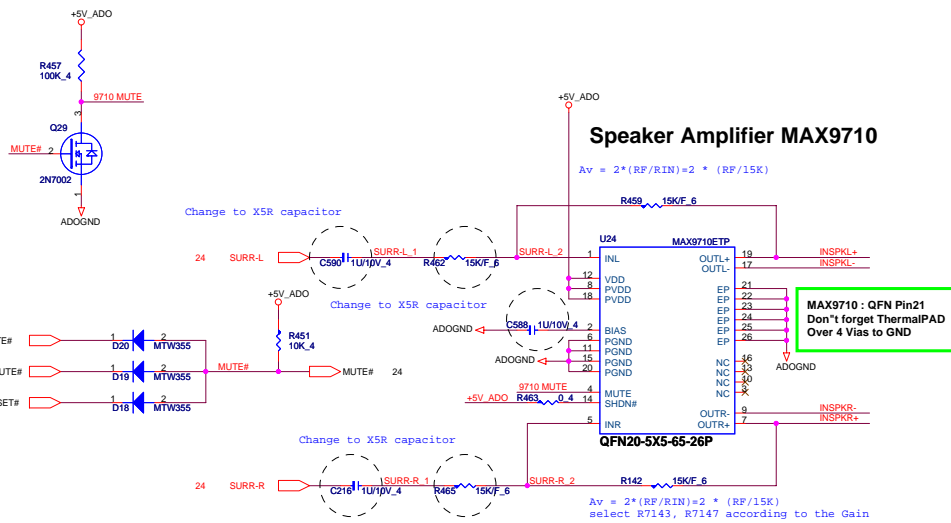
BIA :P/N change to
CH6102K9A19(H=0.85)



For MDC Module

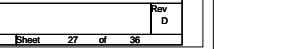
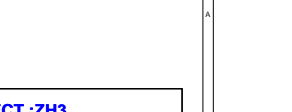
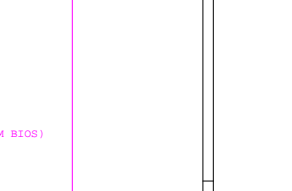
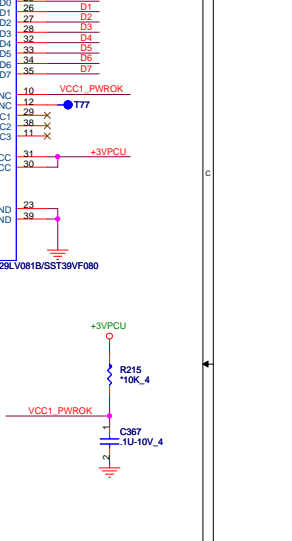
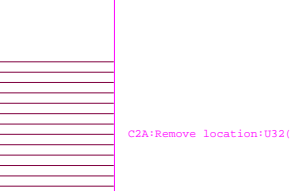
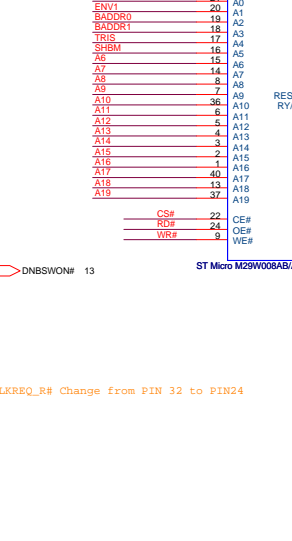
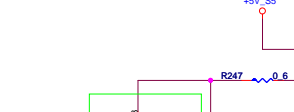
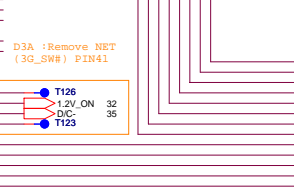
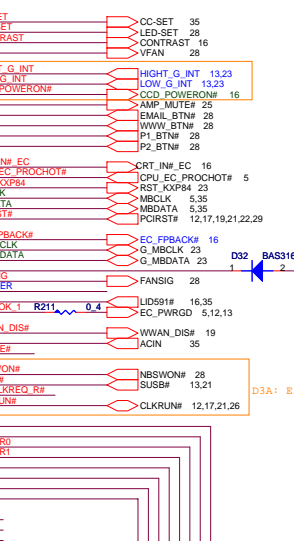
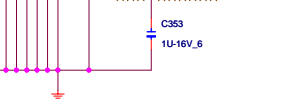
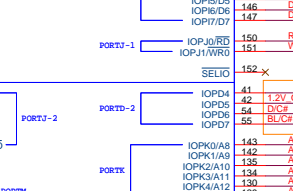
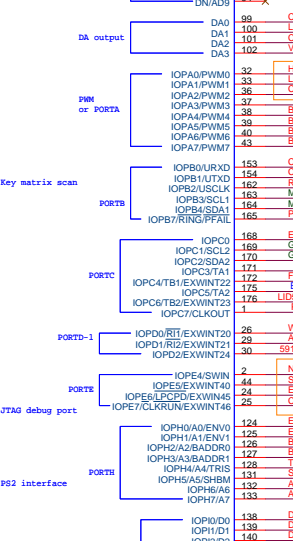
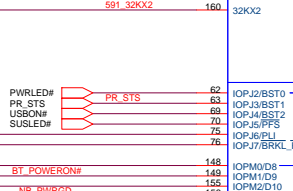
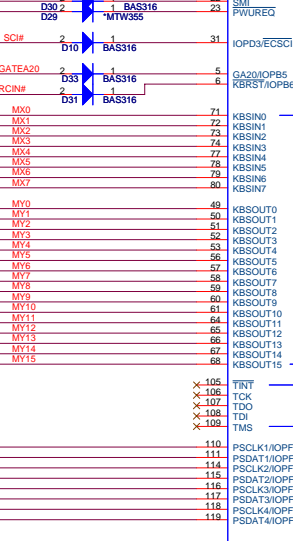
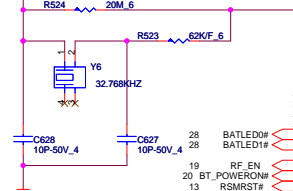
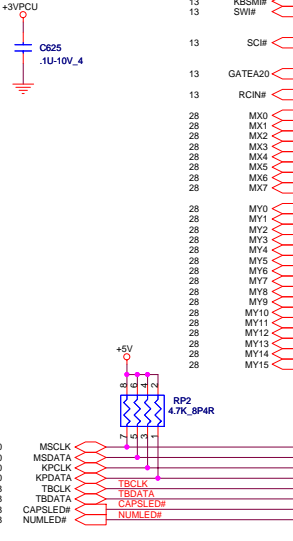
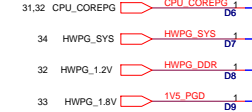
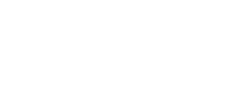
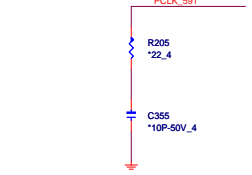
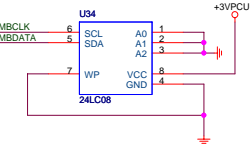
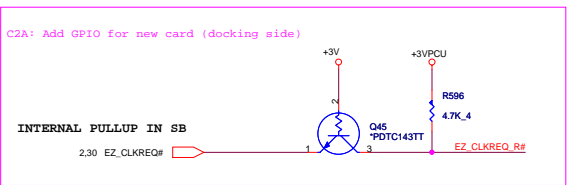


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I/O Address		
BAADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCF0BAH, HCF0BAL) (HCF0BAH, HCF0BAL+1)	
1 1	Reserved	

WIRELESS_SW#	R512	4.7K_4
BLUETOOTH_SW#	R513	4.7K_4

ENV0	21	A0	D0
ENV1	20	A1	D1
BADDR0	19	A2	D2
BADDR1	18	A3	D3
TRIS	17	A4	D4
SHBM	16	A5	D5
MBCLK	15	A6	D6
MBDATA	14	A7	D7
CC-SET	35		
LED-SET	28		
CONTRAST	16		
VFAN	28		
HIGHT G_INT	13,23		
LOW G_INT	13,23		
CCD_POWERON#	16		
AMP_MUTE#	25		
BT1#	36	A10	
BT2#	39	A11	
BT3#	40	A12	
BT4#	43	A13	
CRT_IN#	16	A14	
CPU_EC_PROCHOT#	5	A15	
RST_KXP84	23	A16	
MBCLK	5,35	A17	
MBDATA	12,17,19,21,22,29	A18	
PCIRST#	12,17,19,21,22,29	A19	
EC_FBACK#	16		
G_MBCLK	23		
G_MBDATA	23		
FANSIG	28		
BUZZER	16,35		
UDS9#	5,12,13		
PWROK	1		
WWAN_DIS#	19		
ACIN	35		
SUSB#	28		
CLKRUN#	12,17,21,26		
ENV0	124		
ENV1	125		
BADDR0	126		
BADDR1	127		
TRIS	128		
SHBM	131		
IOPH0/A0/ENV0	132		
IOPH1/A1/ENV1	133		
IOPH2/A2/BADDR0	134		
IOPH3/A3/BADDR1	135		
IOPH4/A4/TRIS	136		
IOPH5/A5/SHBM	137		
IOPH6/A6	138		
IOPH7/A7	139		
IOPI0/D0	140		
IOPI1/D1	141		
IOPI2/D2	142		
IOPI3/D3	143		
IOPI4/D4	144		
IOPI5/D5	145		
IOPI6/D6	146		
IOPI7/D7	147		
IOPI0/RD	148		
IOPI1/WR	149		
IOPI2/BS0	150		
IOPI3/BS1	151		
IOPI4/BS2	152		
IOPI5/PFS	153		
IOPI6/PL	154		
IOPI7/BRK1_RST0	155		
IOPI0/A8	156		
IOPI1/A9	157		
IOPI2/A10	158		
IOPI3/A11	159		
IOPI4/A12	160		
IOPI5/A13	161		
IOPI6/A14	162		
IOPI7/A15	163		
IOPI0/A16	164		
IOPI1/A17	165		
IOPI2/A18	166		
IOPI3/A19	167		
IOPI4/WR1	168		

RESET#	10	VCC1_PWRON
RYBY#	12	
NC1	28	
NC2	38	
NC3	11	
VCC	30	
GND	39	

CE#	22	
OE#	24	
WE#	25	

CE#	22	
OE#	24	
WE#	25	

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CE#	22	
OE#	24	
WE#	25	

PROJECT :ZH3

Quanta Computer Inc.

Size Document Number 97551 & FLASH

Date: Tuesday, June 27, 2006 Sheet 27 of 36

5 4 3 2 1

REV B P/N:FT CHANGE

3V3VPCU

modify D

10 9 8 7 6 5 4 3 2 1

RP5

MY15 MY14 MY13 MY12 MY11 MY10 MY9 MY8 MY7 MY6 MY5 MY4 MY3 MY2 MY1

10 9 8 7 6 5 4 3 2 1

RP6

MY15 MY14 MY13 MY12 MY11 MY10 MY9 MY8 MY7 MY6 MY5 MY4 MY3 MY2 MY1

10 9 8 7 6 5 4 3 2 1

RP4

MX6 MX5 MX4 MX3 MX2 MX1 MY0 MY1 MX0

10 9 8 7 6 5 4 3 2 1

RP3

MX6 MX5 MX4 MX3 MX2 MX1 MY0 MY1 MX0

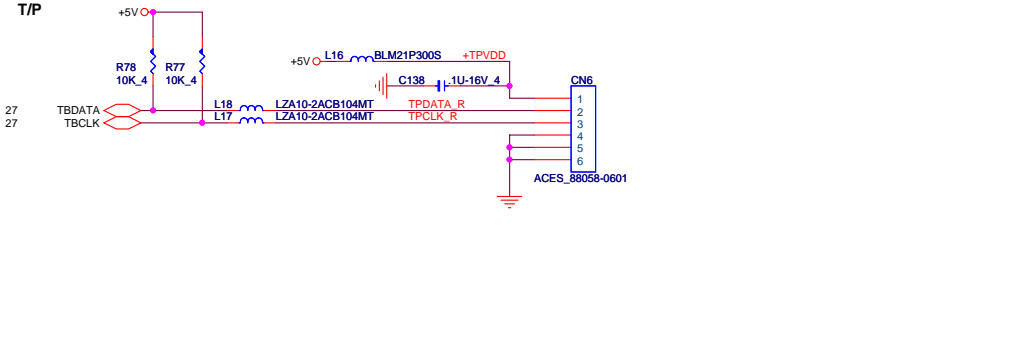
220P-50V, 8P4C

220P-50V, 8P4C

220P-50V, 8P4C

220P-50V, 8P4C

ACS_88264-2501

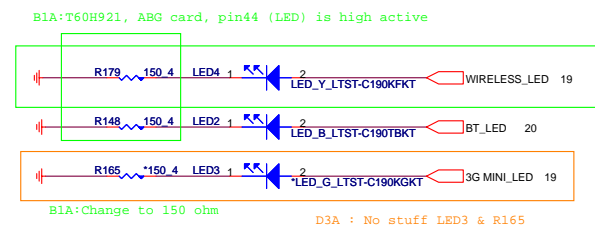


Pinout diagram for the SW_BOARD_M0 connector. The diagram shows a 16-pin header with pins numbered 1 to 16. The pins are connected to various components:

- Pin 1: +3V
- Pin 2: NUMLED
- Pin 3: CAPSLD
- Pin 4: PWRLEDDC
- Pin 5: EMAIL_LED
- Pin 6: WWW_BTN#
- Pin 7: EMAIL_BTN#
- Pin 8: P1_BTN#
- Pin 9: P2_BTN#
- Pin 10: HDD_LED
- Pin 11: GND
- Pin 12: GND
- Pin 13: GND
- Pin 14: GND
- Pin 15: GND
- Pin 16: GND

The connector is labeled SW_BOARD_M0.

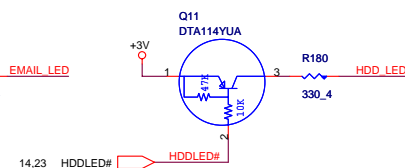
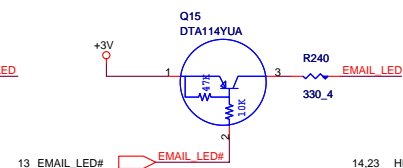
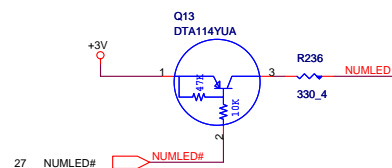
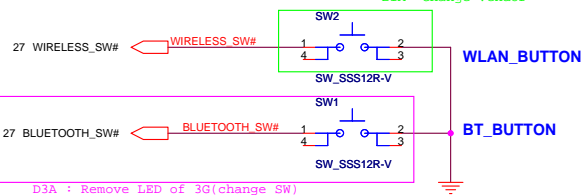
Diagram illustrating the connection of NBSWON# to MB. The signal NBSWON# is connected to pin 2 of connector CN32. Pin 1 is connected to PWRLEDVCC. Pin 3 is connected to ground. Pin 4 is connected to ground. The diagram is labeled ACES_85201-0405L.



```

BlA: Modify, Solve issue of LED.
Change PIN3 to WIRELESS_SW#
Change PIN4 to float
                                BlA :Change vendor

```



B1A: Change from +5V to +5V_S5
C2A: Change from +5V_S5 to +5VUS

D3A : Remove R201

20 MIL

B1A: Add R589

5V

5VUS

27 LED-SET

R597 0.6

R293 0.6

U6

VIN

VO

GND

VEN

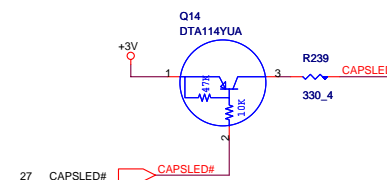
VSET

GND

G995

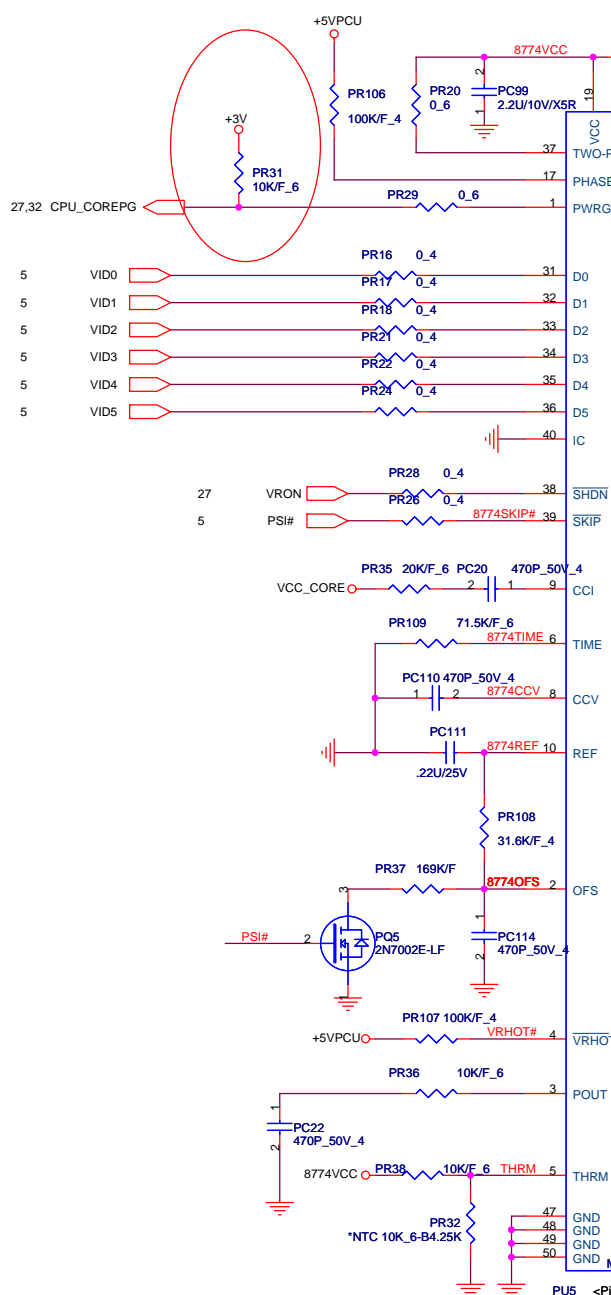
R589 47/F 6 PWRLEDVCC

The schematic diagram illustrates the fan speed control circuit. It features a +5V supply connected to a MOSFET Q2 (AO3403) through a resistor R35 (10K_6). The MOSFET's gate is connected to the +5V supply, and its drain is connected to the TH_FAN_POWER pin. The MOSFET's source is connected to ground. The TH_FAN_POWER pin is connected to a 30 MIL trace, which is then connected to the FANSIG pin. The FANSIG pin is connected to a capacitor C507 (01U-16V_4) and a capacitor C508 (01U-16V_4). The FANSIG pin is also connected to a resistor R297 (10K_4) and a +3V supply. The +3V supply is connected to the FAN_CON pin. The FAN_CON pin is connected to a fan speed sensor FAN_CON. The FAN_CON pin is also connected to a resistor R296 (0.4_1) and a V_FAN pin. The V_FAN pin is connected to the U13 (G995) chip. The U13 chip has a VSET pin connected to ground and a V_FAN pin connected to the V_FAN pin. The U13 chip also has a V_O pin connected to ground and a V_EN pin connected to ground. The U13 chip is connected to the FANSIG pin and the FAN_CON pin.

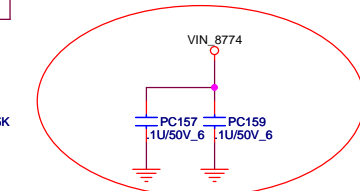
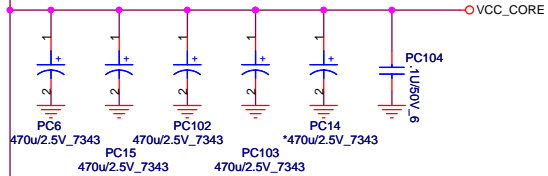
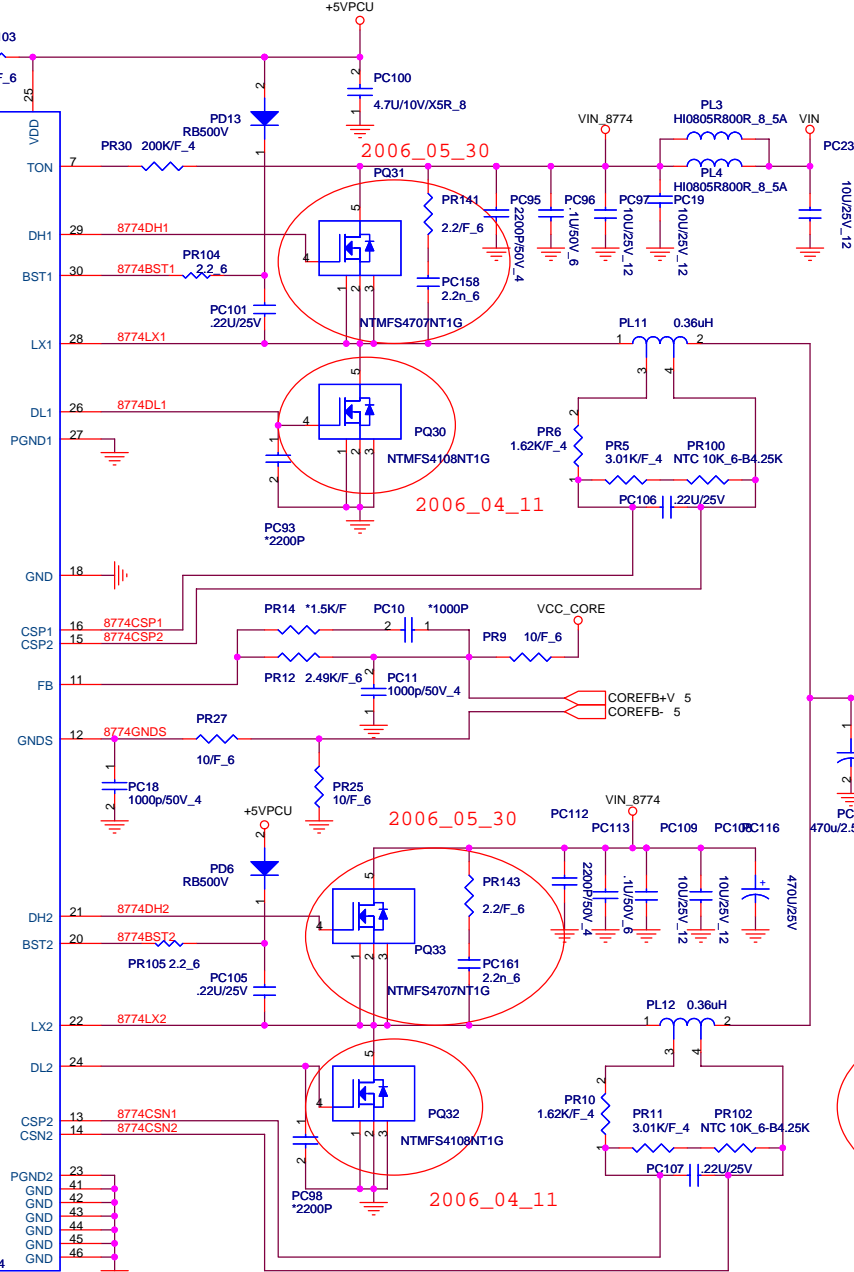


Size	Document Number LED & SW & KB & TP & FAN	Rev D
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2006_03_06 for AMD

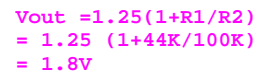


PUS <Pin Numbers Visible>
B1A:PUS Change footprint to -50P



2006-0417
For EMI

change from NCP5214 to SC480IMLTRT



Change list

Item	Fixed Issue	Modify List	Schematic Rev.	PG#	
1	New card issue.	NC_EN# connect the PIN4 & PIN17 of CN2 and PIN11 & PIN12 of CN14	B	13,31	
2	New card issue.	Change from USB8 to USB5 for new card,	B	13,31	
3	Lan issue.	Signal change from INTF to INTG	B	12,17	
4	INT MIC issue.	CN8.2 change from MIC2_INT to MIC_GND	B	25	
5	Wireless LED issue.	SW2.1 change from GND to wireless_sw#, SW2.2 change from wireless_sw# to GND.PIN3,4 is float	B	28	
6	DVI issue	Q40.1 change from PHL_DATA to DDC_DATA	B	29,30	
7	RAMP test				
8					
9					
10					
1					
2					
3					
4					
5					
6					
7					
8					
1					
2					
3					